Appl. No. 10/738,472
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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Withdrawn): A memory device with a vertical transistor and a trench capacitor, comprising:

a substrate with at least one deep trench;

a trench capacitor disposed in the bottom of the deep trench;

a conducting wire disposed on the trench capacitor;

a trench top insulating layer disposed on the conducting wire, in which the top trench insulating layer consists of a first insulating layer and a second insulating layer surrounded by the first insulating layer; and

a control gate disposed on the trench top insulating layer.

Claim 2 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 1, further comprising a buried strap in the substrate beside the conducting wire to electrically connect the control gate as a drain.

Claim 3 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 1, further comprising a doped area in the substrate beside the control gate as a source.

Claim 4 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 1, wherein the first insulating layer is an oxide-nitride layer.

Claim 5 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 4, wherein a thickness of the oxide layer is 5 to 10Å.

Claim 6 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 4, wherein a thickness of the nitride layer is 40 to 50Å.

Claim 7 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of

claim 4, wherein the oxide layer is formed by thermal oxidation.

Claim 8 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 4, wherein the nitride layer is formed by CVD.

Claim 9 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 1, wherein the second insulating layer is BPSG, PSG, NSG or TEOS oxide layer.

Claim 10 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 1, wherein a thickness of the second insulating layer is 200 to 400Å.

Claim 11 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 1, wherein the second insulating layer is formed by LPCVD.

Claim 12 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 1, wherein the conducting wire has a first conducting layer and a second conducting layer , the conducting wire and the substrate are isolated by a circular insulating layer, and the second conducting layer surrounds the first conducting layer and the circular insulating layer .

Claim 13 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 12, wherein the first conducting layer is a doped poly layer or a doped epi-silicon layer.

Claim 14 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 12, wherein the second conducting layer is a poly layer or a epi-silicon layer.

Claim 15 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 12, wherein the circular insulating layer is a silicon oxide layer.

Claim 16 (Withdrawn): The memory device with a vertical transistor and a trench capacitor of claim 1, wherein the control gate consists of a gate conducting layer and a gate oxide layer, and the gate conducting layer consists of a poly layer, a WSi layer, a metal layer, or a composite thereof.

Claim 17 (Original): A method for fabricating a memory device with a vertical transistor and a trench capacitor, comprising:

providing a substrate;

forming at least one deep trench in the substrate;

forming a trench capacitor in the bottom of the deep trench;

forming a conducting wire on the trench capacitor;

forming a trench top insulating layer on the conducting wire, in which the trench top insulating layer consists of a first insulating layer and a second insulating layer surrounded by the first insulating layer; and

forming a control gate on the trench top insulating layer.

Claim 18 (Original): The method for fabricating a memory device with a vertical transistor and a trench capacitor of claim 17, further comprising a buried strap in the substrate beside the conducting wire to electrically connect the control gate as a drain.

Claim 19 (Original): The memory device with a vertical transistor and a trench capacitor of claim 17, further comprising a doped area in the substrate beside the control gate as a source.

Claim 20 (Original): The memory device with a vertical transistor and a trench capacitor of claim 17, wherein the first insulating layer is an oxide-nitride layer.

Claim 21 (Original): The memory device with a vertical transistor and a trench capacitor of claim 20, wherein a thickness of the oxide layer is 5 to 10Å.

Claim 22 (Original): The memory device with a vertical transistor and a trench capacitor of claim 20, wherein a thickness of the nitride layer is 40 to 50Å.

Claim 23 (Original): The memory device with a vertical transistor and a trench capacitor of claim 20, wherein the oxide layer is formed by thermal oxidation.

Claim 24 (Original): The memory device with a vertical transistor and a trench capacitor of claim

20, wherein the nitride layer is formed by CVD.

Claim 25 (Original): The memory device with a vertical transistor and a trench capacitor of claim 17, wherein the second insulating layer is BPSG, PSG, NSG or TEOS oxide layer.

Claim 26 (Original): The memory device with a vertical transistor and a trench capacitor of claim 17, wherein a thickness of the second insulating layer is 200 to 400Å.

Claim 27 (Original): The memory device with a vertical transistor and a trench capacitor of claim 17, wherein the second insulating layer is formed by LPCVD.

Claim 28 (Currently Amended): The memory device with a vertical transistor and a trench capacitor of claim 17, wherein the conducting wire has a first conducting layer and a second conducting layer, the first conducting layer of the conducting wire and the substrate are isolated by a circular insulating layer, and the second conducting layer lies on ~~surrounds~~ the first conducting layer and the circular insulating layer .

Claim 29 (Original): The memory device with a vertical transistor and a trench capacitor of claim 28, wherein the first conducting layer is a doped poly layer or a doped epi-silicon layer.

Claim 30 (Original): The memory device with a vertical transistor and a trench capacitor of claim 28, wherein the second conducting layer is a poly layer or an epi-silicon layer.

Claim 31 (Original): The memory device with a vertical transistor and a trench capacitor of claim 28, wherein the circular insulating layer is a silicon oxide layer.

Claim 32 (Original): The memory device with a vertical transistor and a trench capacitor of claim 28, wherein the control gate consists of a gate conducting layer and a gate oxide layer, and the gate conducting layer consists of a poly layer, a WSi layer, a metal layer, or a composite thereof.

Claim 33 (Currently Amended): A method for fabricating a memory device with a vertical

transistor and a trench capacitor, comprising:

providing a substrate;

forming at least one deep trench in the substrate;

forming a trench capacitor in the bottom of the deep trench;

forming [[a]] an insulating layer on the trench capacitor, a sidewall of the deep trench, and the substrate;

etching the insulating layer until the insulating layer on the trench capacitor and the substrate is removed to form a circular insulating layer on the sidewall of the deep trench;

filling a first conducting layer in the deep trench;

etching the first conducting layer to expose the circular insulating layer;

etching the circular insulating layer to below the first conducting layer in the deep trench;

forming a second conducting layer on the first conducting layer, the circular insulating layer, the sidewall of the deep trench, and the substrate;

partially etching the second conducting layer to remove the second conducting layer on the sidewall of the deep trench and the substrate to leave the second conducting layer coning the first conducting layer and the circular insulating layer, in which a conducting wire consists of the first conducting layer and the second conducting layer;

conformably forming a first insulating layer on the second conducting layer, the sidewall of the deep trench, and the substrate;

partially etching the first insulating layer to remove the first insulating layer on the second conducting layer and the substrate to form a spacer on the sidewall of the deep trench;

filling a second insulating layer in the deep trench;

etching the second insulating layer to expose the first insulating layer;

etching the first insulating layer to remove the first insulating layer on the sidewall above the second insulating layer to leave ~~the second~~ a remaining first insulating layer on a sidewall of the second insulating layer, in which a trench top insulating layer consists of the remaining first insulating layer and the second insulating layer; and

forming a control gate on the trench top insulating layer.

Claim 34 (Original): The method for fabricating a memory device with a vertical transistor and a trench capacitor of claim 33, further comprising a buried strap in the substrate beside the conducting wire to electrically connect the control gate as a drain.

35 (Original): The memory device with a vertical transistor and a trench capacitor of claim 33, further comprising a doped area in the substrate beside the control gate as a source.

36 (Original): The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the first insulating layer is an oxide-nitride layer.

Claim 37 (Original): The memory device with a vertical transistor and a trench capacitor of claim 36, wherein a thickness of the oxide layer is 5 to 10Å.

Claim 38 (Original): The memory device with a vertical transistor and a trench capacitor of claim 36, wherein a thickness of the nitride layer is 40 to 50Å.

Claim 39 (Original): The memory device with a vertical transistor and a trench capacitor of claim 36, wherein the oxide layer is formed by thermal oxidation.

Claim 40 (Original): The memory device with a vertical transistor and a trench capacitor of claim 36, wherein the nitride layer is formed by CVD.

Claim 41 (Original): The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the second insulating layer is BPSG, PSG, NSG or TEOS oxide layer.

Claim 42 (Original): The memory device with a vertical transistor and a trench capacitor of claim 33, wherein a thickness of the second insulating layer is 200 to 400Å.

Claim 43 (Original): The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the second insulating layer is formed by LPCVD.

Claim 44 (Original): The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the first conducting layer is a doped poly layer or a doped epi-silicon layer.

Claim 45 (Original): The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the second conducting layer is a poly layer or an epi-silicon layer.

Claim 46 (Original): The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the circular insulating layer is a silicon oxide layer.

Claim 47 (Original): The memory device with a vertical transistor and a trench capacitor of claim 33, wherein the control gate consists of a gate conducting layer and a gate oxide layer, and the gate conducting layer consists of a poly layer, a WSi layer, a metal layer, or a composite thereof.